NOISE AN]) ELECTRICAL CHARACTERIZATION OF COMPLEMENTARY 11H{'J'13ROJLJNCI'1ON FIELD-EFFECT TRANSISTORS (CHFET)

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This paper discusses the electrical properties of the complementary heterojunction field-cfkct transistor (CHFET) at 4 K, including the gate leakage current, the subthreshold transconductance, and the input-referred noise voltage. The CHFET is a GaAs-based transistor analogous in structure and operation to silicon CMOS, and is being explored for possible application in readout electronics operating at 2-4 K. It is shown that CHFET is fully functional at 4 K, with no anomalous behavior, and that the drain current shows the expected dependence on device size and gate voltage. The input-referred noise is on the order of 1 $\mu V/\sqrt{Hz}$ at 100 Hz. The gate current is strongly dependent on the doping at the gate edge, and is on the order of 10-] 4 amps for devices with the lightest doping. A simple multiplexed op-amp is presented, along with its transfer characteristics at 4 K.

INTRODUCTION

The design of systems that include detector focal plane arrays operating at temperatures below 10 K would be greatly simplified by the availability of readout electronics that can operate at the detector temperature. Otherwise, the designer is forced to isolate the electronics in a warmer compartment and run a wire for each sensor in the array from the focal plane cold head to the warmer electronics compartment. These wires carry heat from the electronics compartment to the cold head, increasing the load on the cold head refrigerator or cryogen supply. The wires are also susceptible to cross-talk and to the pickup of noise through electromagnetic induction or microphonics. As the array size increases, these problems become more acute, making this "brute force" method increasingly less attractive. By contrast, if the electronics are placed directly on the cold head with the sensor array, these problems are reduced or eliminated. The sensor array can be bump bonded directly to the associated array of electronics, which reduces the electrical connection between the sensor and electronics to micron lengths, making

electromagnetic and microphonics noise pickup negligible. Also, since the electronics and sensor arc at the same temperature, these connections do not contribute to the heat load. Because the electronics amplify and multiplex the signals from the detectors, there are fewer leads coming off of the cold head for reduced heat conduction, and the amplified signals arc less susceptible to noise.

The major technical challenge involved in building very low temperature electronics is due to the phenomenon of carrier "freeze-out." For semiconductor material that is not heavily doped, it requires a small but finite energy to liberate carriers from the dopant atoms so that they can travel freely through the semiconductor and contribute to conduction. At sufficiently low temperatures, the carriers lack the required energy and arc recaptured by the dopant atoms or other traps. This causes the conductivity of the semiconductor to fall sharply as the temperature is lowered, which results in degraded performance, o r complete device failure, of any transistor that is made of that Semiconductor. Even if the device dots not fail completely, the trapping and de-trapping of carriers causes the conductivity to vary with time, This results in I/f noise and in performance anomalies such as hysteresis.

By far the most popular material system for low power electronics has been silicon complementary mcta{-oxide-semiconductor (CMOS) technology. However, silicon is poorly suited to very low temperature applications. The ionization energies for free carriers in silicon is relatively high. As a result, silicon freezes-out at a relatively high temperature, and it requires very high doping levels to make silicon degenerate. Conventional silicon bipolar transistors cease to function below about 50 K. CMOS transistors can operate to somewhat lower temperatures, but conventional CMOS still exhibits excessive noise and current-voltage anomalies such as kinks and hysteresis below about 20 K. The state-of-the-art CMOS optimized for low temperatures has demonstrated anomaly-free performance and moderate noise levels down to and slightly below 10 K (1). Despite this advance, it is not clear whether silicon technology will be able to meet the requirements oflow-power, low temperature analog electronics.

By contrast, GaAs-based transistors exhibit superior performance at low temperatures. The ionization energy for electrons is much smaller that for silicon, so it freezes-out at a much lower temperature, and becomes degenerate at much lower doping concent rations. In addition, epitaxial growth technology is highly advanced for GaAs-based structures which allows the growth of very pure semiconductor with few background impurities that can act as traps. It also allows the growth of heterojunctions that can separate the carrier charge from traps and dopants. Several groups have begun to explore GaAs-based transistors for low temperature readout electronics applications (2-6). For example, R, Kirschman et. al., have studied commercial and foundry GaAs Junction field-effect transistors (JFETs) and metal-Schottky field-eflcct transistors (MESFETs) at 4 K (2). Also, Kozlowski ct. al., have designed GaAs-based circuits for low temperature readouts (3).

THE STRUCTURE OF THE CHFET

As part of the NASA Sensor Electronics Program, J])], has been studying GaAs-based electronics for readout electronics applications in the 2-4 K temperature range. This has included an investigation of the low-temperature properties of a type of CMOS-like GaAs-based transistor called the complementary heterojunction field-effect transistor (C311'1;'1'). The CHFET was developed by 1 loneywell for high-speed, room-temperature digital applications (7). It has several features, however, that indicate that it might be suitable for very-low temperature operation.

A cross-section of the CHFET is shown in Fig. 1. Starting on a semi-insulating GaAs substrate, molecular beam epitaxy (MBE) is used to grow a GaAs buffer layer, an InGaAs channel, a high aluminum mole-fraction AlGaAs layer, and a thin GaAs cap layer for surface passivation. A WSi gate is deposited and serves to make the source and drain self-aligned. The entire structure can be undoped except for the implanted source and drain which arc degenerately doped, These implants can be either n-type or p-type allowing complementary transistor circuits. The device operates in enhancement mode in a manner analogous to that of silicon CMOS, with the AlGaAs layer playing the role of the oxide. A gate voltage draws electrons or holes into the channel where they are confined vertically by the AlGaAs dielectric. The carriers move laterally, and are collected by the drain. The gate voltage modulates the channel charge density above threshold, and the channel potential below threshold.

The availability of complementary devices is extremely useful in the design of low power electronics. The fact that the structure can be made so that each region of the device is either degenerately doped or undoped makes the device immune to freeze-out. Because the carriers are confined by the heterojunction barrier to a channel that can be undoped, the carriers can have very high mobility, and will see few impurities, traps, or surface states to scatter or trap them, Together these facts indicate that the CHFET offers a good deal of promise as a Iow-power, low-noise device functional at very low t emperat ures.

CURRENT-VOLTAGE CHARACTERISTICS

Two lots of CHFETs were fabricated at 1 loneywell Systems and Research Center and were sent to JPL for characterization. The AlGaAs dielectric layer thickness was 250 Å for these experimental devices, and the aluminum mole fraction was 0.75. As stated in the previous section, it is possible to fabricate the CHFET such that it is entirely undoped except for the source and drain. The devices that were tested, however, were fabricated as part of a larger lot designed for high speed digital applications, and used a

delta-doped layer in the channel in order to make the n-channel and p-channel threshold voltages more symmetric, in addition, some devices also included a well implant. This was a p-type implant for n-channel devices and n-type for p-channel devices.

The current-voltage characteristics both above and below threshold were measured at 4 K using a } IP4145B semiconductor parameter analyzer. The transistor curves for an n-channel and a p-channel device arc shown in Fig. 2. The dependence of the drain current on the gate voltage at 4 K is examined in Fig. 3. The subthreshold current for various size devices is plotted on a log scale. The square root of the current above threshold is plotted on a linear scale. These figures show that the (} IFET operates normally at 4 K without any anomalies, and that the devices exhibit the expected dependence on gate voltage and device sire.

GATE LEAKAGE CURRENT

The gate leakage current was measured with the source and drain grounded using an HP4145B semiconductor parameter analyzer. The gate current for positive and negative gate voltages at various temperatures between 10 K and 290 K is shown in Fig. 4. The gate current has been examined in previous studies and has been shown to bc duc to a combination of fie]d-emission, thcrmionic-field-emission, thcrmionic-emission, and ohmic conduction, each of which is dominant for different values of the temperature and gate voltage (8,9). Below 10 K, the current is dominated by field mission. For reverse gate voltages (negative for n-channel CHFETs), the current is described well by the Fowler-Nordhcim equation. The forward current also appears to bc field emission, but its voltage dependence dots not fit the Fowler-Nordheim dependence. Neither forward or reverse current shows any regular dependence on the gate area or width. Instead, there is a large and seemingly random variation from device to device. When plotted on a semilog scale, the current-vohagc curves for various device tends to cluster, with about 80'% of the devices on any chip showing approximately the same behavior (within an order of magnitude), and with 20% of the devices as outliers, with much higher current levels (greater than two orders of magnitude), This indicates that the gate current may bc dependent on the material, e.g., tunneling through defects, or process dependent, e.g., tunneling from point emitters on the gate edge.

The gate current dots show a strong dependence on the doping level adjacent to the gate edge. Four sets of devices were made froJn the quadrants of onc wafer. Each received a different doping implant. Three of the four received a light well implant before the gate was deposited, which was p-type for the n-channel devices and n-type for the p-channel devices. After the gate was defined, the devices received an implant adjacent to the gate. A gate sidewall spacer was then attached to the gate and the source and drain implants were done. Thus the doping in the sidewall region adjacent to the gate could bc controlled

independent of the source and drain implants, The three quadrants that received the well implant were fabricated with heavy, moderate, and light sidewall region doping. The quadrant that received no well implant was fabricated with moderate sidewall region doping. The gate currents for a typical device from each quadrant arc compared in Fig. 5. The current for the device with heavy sidewall region doping is much larger that the others. The device with the light sidewall region doping has the smallest current. The devices with the moderate sidewall doping had gate currents which were comparable to but slightly greater than that with the light doping. The device with moderate sidewall doping that received the well implant showed smaller leakage current than the device than did not receive a well implant.

The gate current and drain current for the device with the light sidewall doping is shown in Fig. 6. The data represented by the solid lines were rccordcd with the } IP4145B parameter analyzer which has a sensitivity of 1 pA. A Keithley 617 electrometer was used in the integrating mode to measure the gate current down to about 10-] 4 amps. This data is plotted as discrete circles in Fig. 5. It can be seen from the subthreshold drain current data that it requires a gate voltage about 0.85 V to bias the device at about 10 nA, which is a reasonable value of bias current to use in low-power readout circuit applications. At this gate voltage the gate leakage current is on the order of 10-14 amps,

THE NOISE VOLTAGE

The input-referred noise voltage was measured using the circuit shown in Fig. 7. The differential amplifier is used to feed back a signal to the gate that keeps the source current constant. The voltage at the output of the amplifier directly provides an amplified replica of the input-referred noise. The noise voltage of three different size n-channel CHFETs, and for 50x50 μm CHFETs with and without a well implant, are shown in Fig. 8. The voltage noise of the largest device without the well implant is approximately 1 $\mu V/\sqrt{Hz}$ at 100117,. The noise decreases with increasing device size, an effect that has been observed in most types of transistors. The noise is increased by the addition of the well implant. This is expected, since additional dopants tend to increase the trapping and scattering of carriers. The noise was also measured as a function of the temperature, drain bias current, and source-drain voltage. None of these had a very significant effect. For some reason, many of the devices showed a peak in the noise at approximately 501 Iz. Some sort of pickup is suspected, but its origin has not yet been found and is still under investigation.

CHFET MULTIPLEXERS

Several different simple 8x 1 multiplexer circuits were also fabricated and tested at 4 K, In each of these a voltage could bc stored on eight capacitors that simulated a small linear array of detectors. Addressable readout electronics were connected to each capacitor and to common output circuitry which included a source follower output driver. Most of these circuits did not operate properly at 4 K. The p-channel CHFETs used to reset the capacitor voltage appeared to exhibit high leakage current from the drain to the gate and source. As a result, the output was influenced by the reset voltage and reset gate enable. P-channel CHFETs were also used in the cell select of most of the circuits, and the leakage of the p-channel devices made it impossible to disable the devices completely. It was not possible to demonstrate the multiplexing action in these devices.

Onc circuit did function, although with limited performance. This circuit consisted of a multiplexed array of operational amplifiers which were enabled by sending a bias voltage signal to the n-channel current source of the differential pair in the selected cell. Although the failure of the p-channel CHFETs still made it impossible to turn off the capacitor reset voltage completely, and probably reduced the impedance of the inverter load, it was possible to scc both inverting and non-inverting action in the device.

This circuit, called the switched op-amp multiplexer, consists of eight differential pairs, each connected to an addressable pair source. The drain of the inverting transistor of each pair is connected to a common p-channel active load. The output voltage is buffered through an n-channel source follower connected to an n-channel current source transistor. A circuit schematic for the switched op-amp multiplexer along with the inverting transfer characteristics for each cell measured at 4 K arc shown in Fig. 9. The voltage gain at 4 K is approximately 250.

SUMMARY

The CHFET has been shown to bc completely functional at 4 K, with no anomalies or hysteresis. It has a clean subthreshold current-voltage characteristic and allows the capability of complementary devices. The gat c leakage is strongly dependent on the doping concentration in the region adjacent to the gate, and a CHFET using a sidewall spacer and light sidewall region doping had a gate leakage current of approximately 10-14 amps for gate voltages that biased the device in the subthreshold region. The noise voltage for the CHFETs is on the order of 1 $\mu V/\sqrt{Hz}$ at 100 Hz. It increases as the device size is reduced, or with the addition of a well implant. A multiplexed op-amp using CHFETs was designed, and was functional at 4 K,

While the capability of complementary logic and anomaly free performance at low temperatures make the CHFET potentially attractive for low-power, low temperature circuitry, the gate leakage is still too high for some applications, and the noise is prohibitively high for most readout applications. Further improvement is necessary to make the (111;1;3' suitable for readout applications below 4 K.

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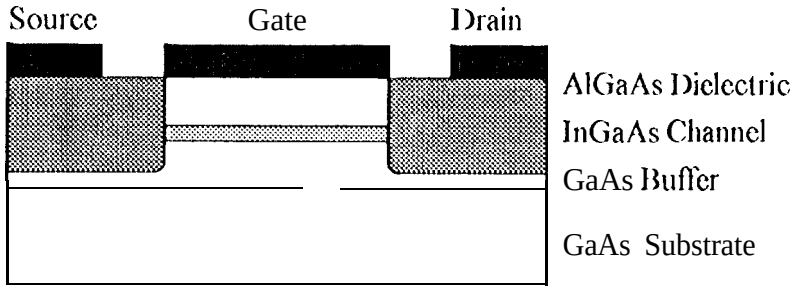

Fig. 1: A cross-section of the complementary heterojunction field effect transistor (CHFET). The entire structure can be undoped except for the source and drain implants, which are degenerately doped.

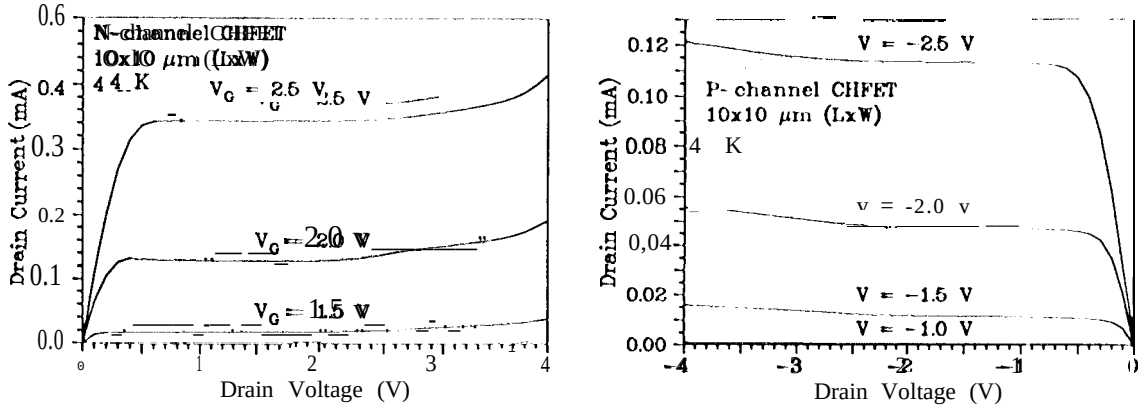

Fig. 2: The transistor curves for an n-channel and p-channel CHFET

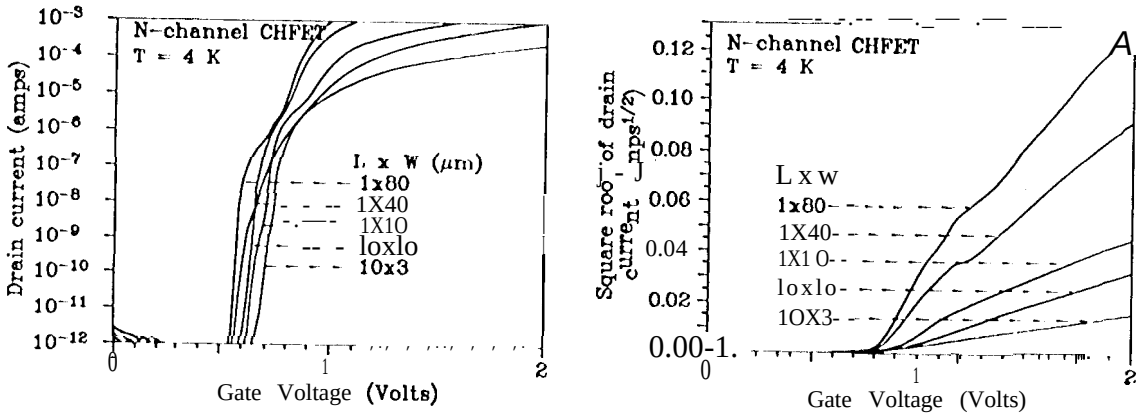

Fig. 3: The dependence of the drain current on the gate voltage, in the subthreshold region and above threshold (plotted as $\sqrt{I}$ vs. V_g).

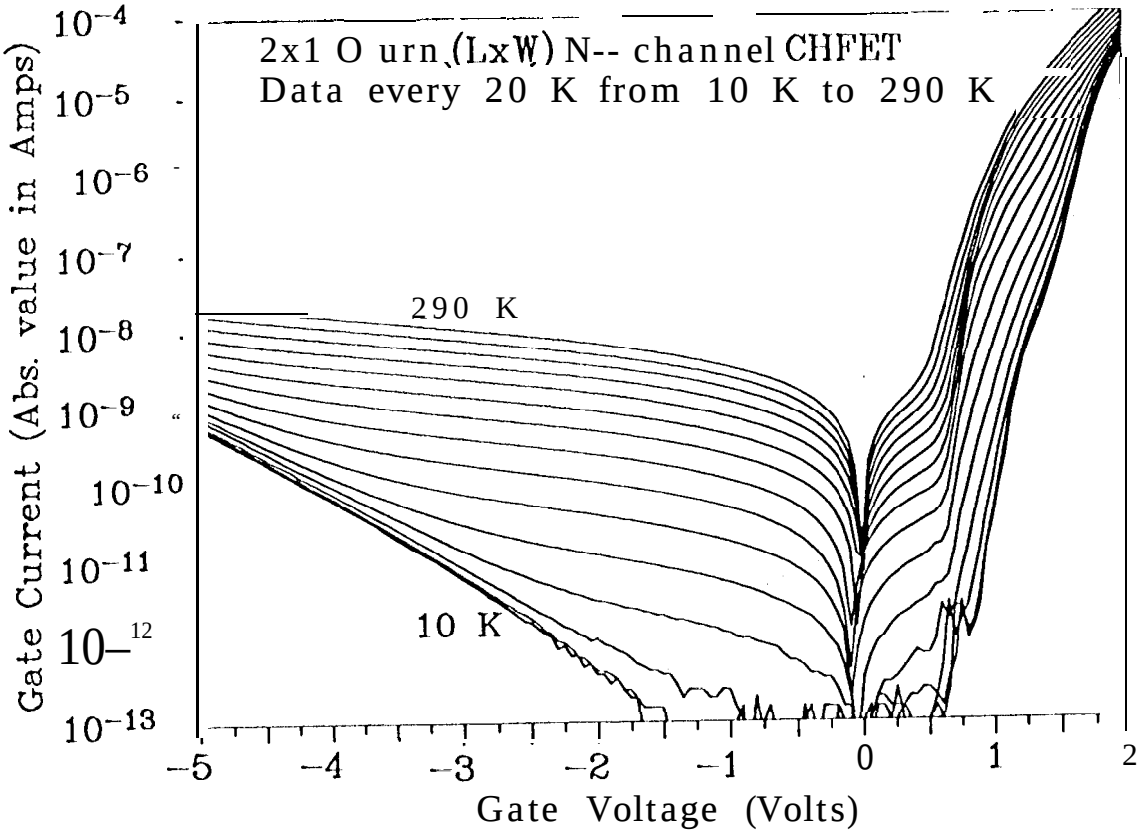

Fig. 4: The gate leakage current vs. gate voltage for temperatures between 10 K and 290 K

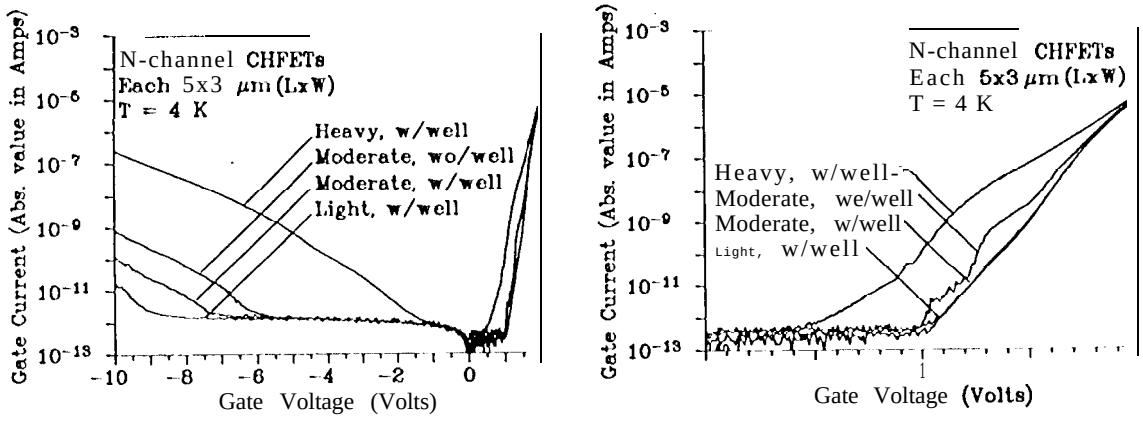

Fig. 5: The gate current vs. gate voltage for different doping concentrations in the sidewall region adjacent to the gate, and for devices with and without a well implant.

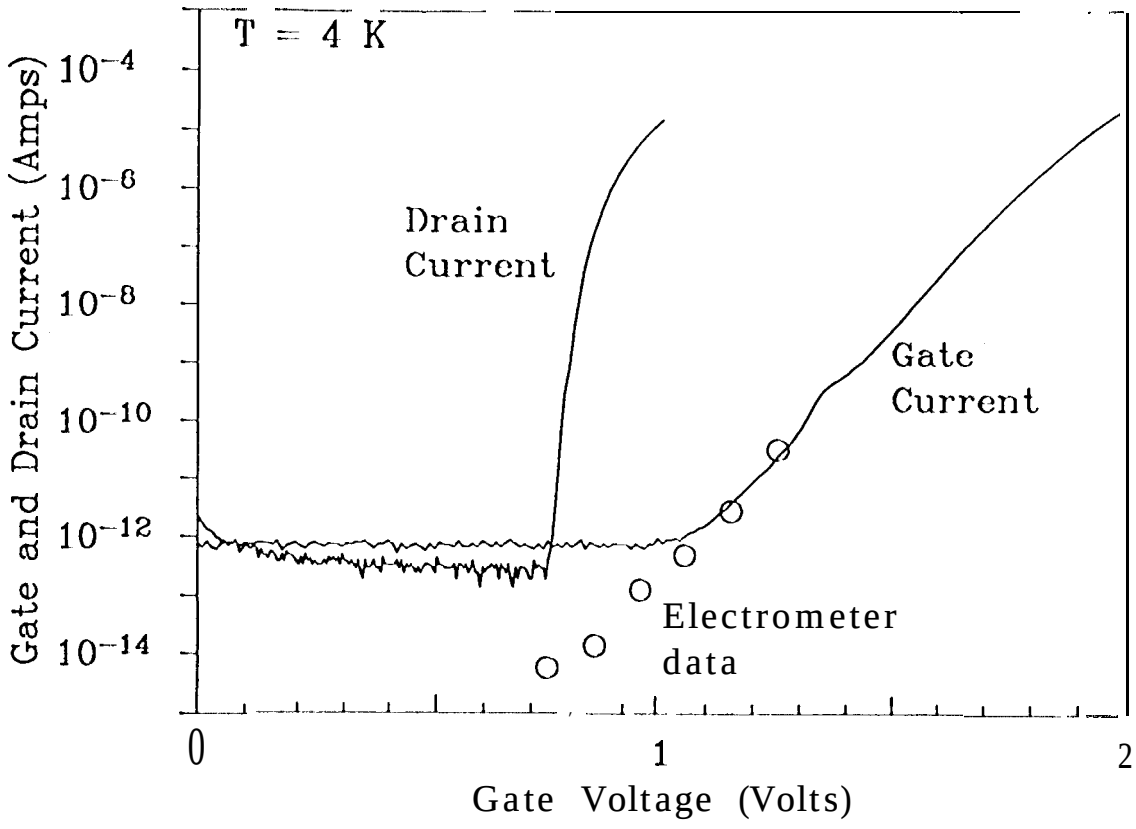

Fig. 6: comparison of the drain current and the gate current in a CHFET with a lightly doped sidewall region and no well implant, The circles arc points taken with a Kcithlcy617 electrometer in the integrating (coulomb) mode,

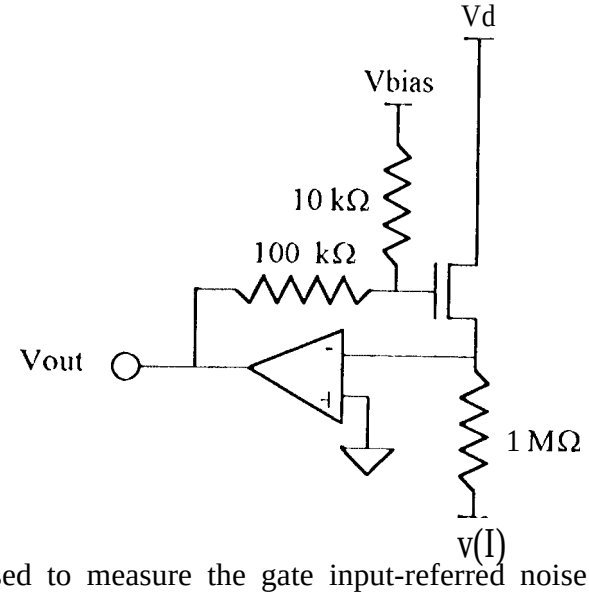

Fig. 7: The circuit used to measure the gate input-referred noise of the CHFETs. The differential amplifier is a PAR 113 preamp.

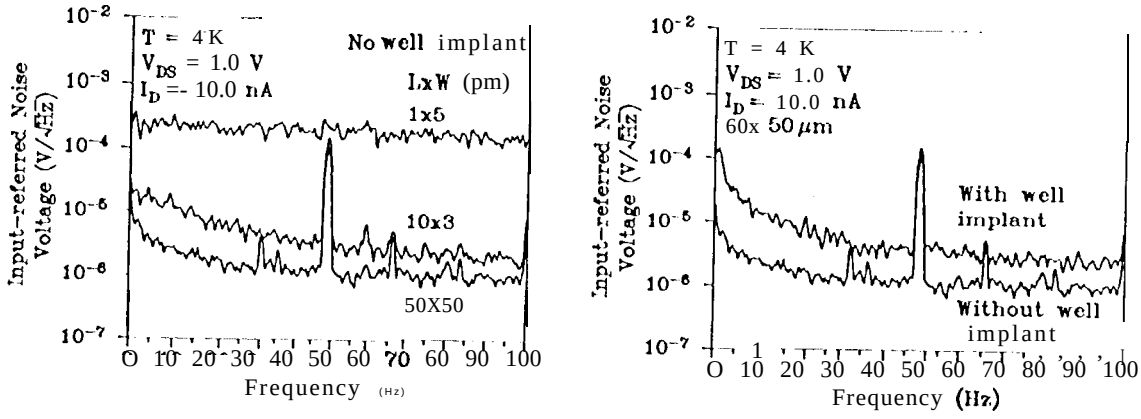

Fig. 8: A comparison of the input-referred noise voltage for devices of different sizes and for devices with and without a well implant.

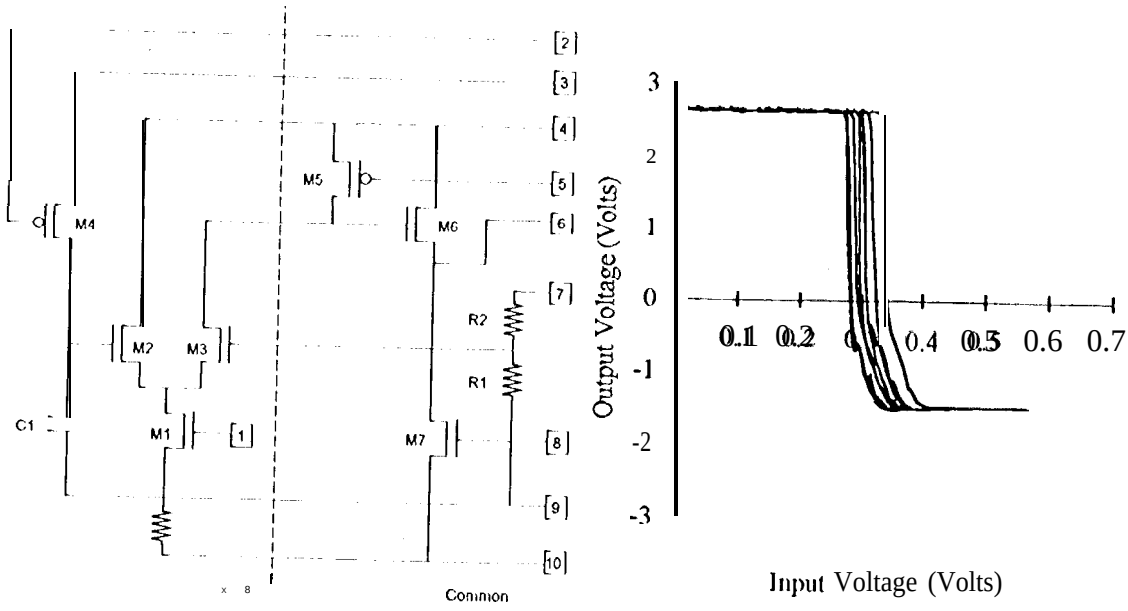

Fig. 9: The circuit schematic for a CHFET 8x 1 switched op-amp multiplexer and the inverting transfer characteristics of each cell taken at 4 K.